

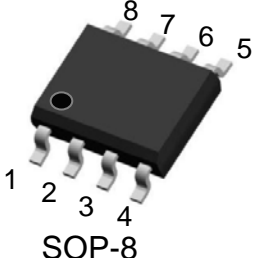
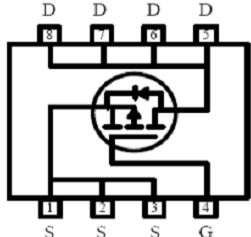
P-Channel Enhancement-Mode MOSFET (-30V, -15A)

PRODUCT SUMMARY

V_{DSS}	I_D	$R_{DS(on)}$ (m Ω)TYP
-30V	-15A	9 @ $V_{GS} = -10V, I_D = -15A$
		15 @ $V_{GS} = -4.5V, I_D = -8A$

Features

- Advanced Trench Process Technology
- High Density Cell Design for Ultra Low On-Resistance
- Fully Characterized Avalanche Voltage and Current
- Improved Shoot-Through FOM
- Lead (Pb) -free and halogen-free

 <p>SOP-8</p>		<p>Pin1/2/3: Source Pin4: Gate Pin5/6/7/8: Drain</p>	TOP Marking
			<p>4 4 1 1 part number XXXXXX ID CODE</p>

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Rated	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current (Continuous)	-15	A
I_{DM}	Drain Current (Pulsed) ^a	-80	A
P_D	Total Power Dissipation @ $T_A = 25^\circ\text{C}$	3.0	W
E_{AS} ^b	Avalanche Energy, Single pulse ($L = 0.3\text{mH}$)	100	mJ
I_S	Maximum Diode Forward Current	-2.6	A
T_j, T_{stg}	Operating Junction and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
R_{QJA}	Maximum Junction-to-Ambient ($t \leq 10\text{s}$) ^c	40	$^\circ\text{C/W}$
	Maximum Junction-to-Ambient (Steady State) ^c	75	$^\circ\text{C/W}$

a: Repetitive Rating: Pulse width limited by the maximum junction temperature.

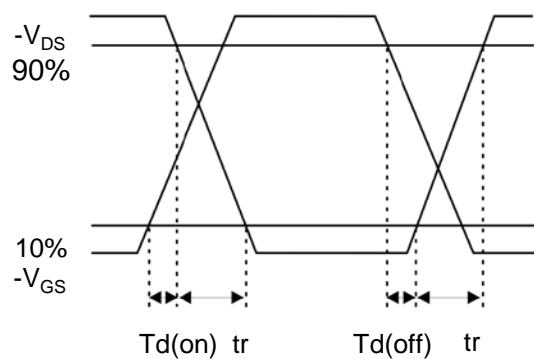
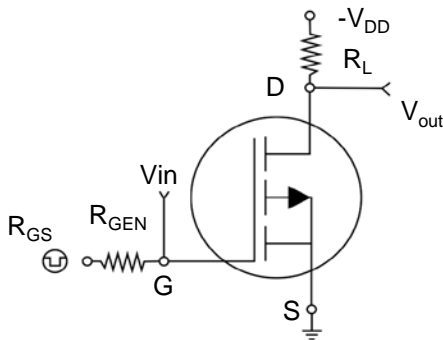
b: Surface Mounted on 1in² pad area, $t < 10\text{sec}$.

c: 1-in² 2oz Cu PCB board

Electrical Characteristics (T_A=25°C, unless otherwise noted)

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
• Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V	-	-	-1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
• On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250uA	-1	-1.3	-2	V
R _{DS(on)}	Drain-Source On-State Resistance	V _{GS} =-10V, I _D =-15A	-	9	12	mΩ
		V _{GS} =-4.5V, I _D =-8A	-	15	23	
• Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	-	2860	-	PF
C _{oss}	Output Capacitance		-	420	-	
C _{rss}	Reverse Transfer Capacitance		-	265	-	
• Switching Characteristics						
Q _g	Total Gate Charge	V _{DS} =-15V, I _D =-5.3A, V _{GS} =-10V	-	47	-	nC
Q _{gs}	Gate-Source Charge		-	11	-	
Q _{gd}	Gate-Drain Charge		-	13	-	
t _{d(on)}	Turn-on Delay Time	V _{DD} =-15V, R _L =5Ω, I _D =-3A, V _{GEN} =-10V, R _G =6Ω	-	15	-	nS
t _r	Turn-on Rise Time		-	11	-	
t _{d(off)}	Turn-off Delay Time		-	44	-	
t _f	Turn-off Fall Time		-	21	-	
• Drain-Source Diode Characteristics						
V _{SD}	Drain-Source Diode Forward	V _{GS} =0V, I _S =-2.0A	-	-	-1.3	V

Note: Pulse Test: Pulse Width ≤ 300us, Duty Cycle ≤ 2%



Switching Test Circuit and Switching Waveforms

Typical Characteristics Curves ($T_A=25^\circ\text{C}$, unless otherwise note)

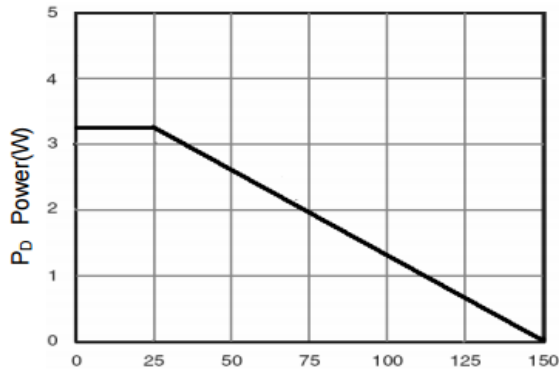


Figure 1 Power Dissipation

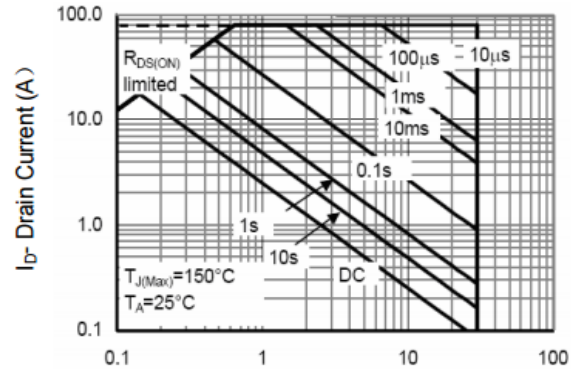


Figure 2 Safe Operation Area

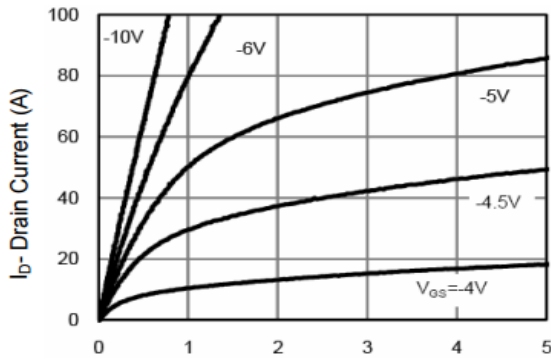


Figure 3 Output Characteristics

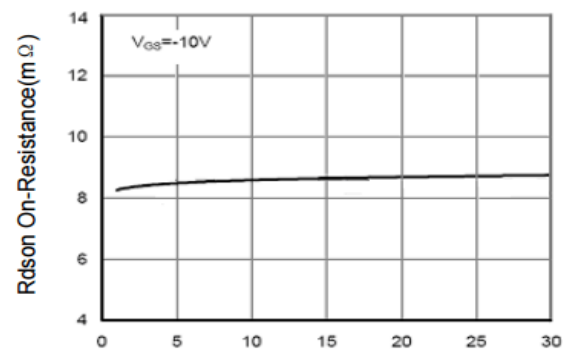


Figure 4 Drain-Source On-Resistance

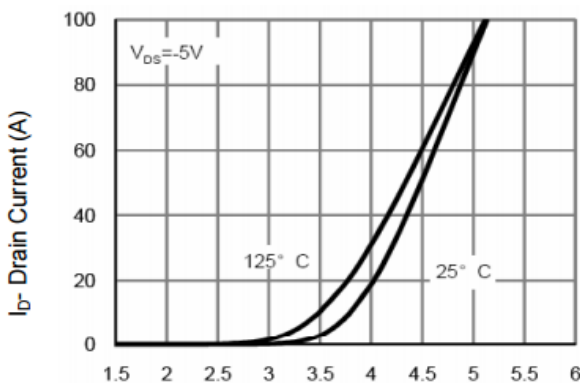


Figure 5 Transfer Characteristics

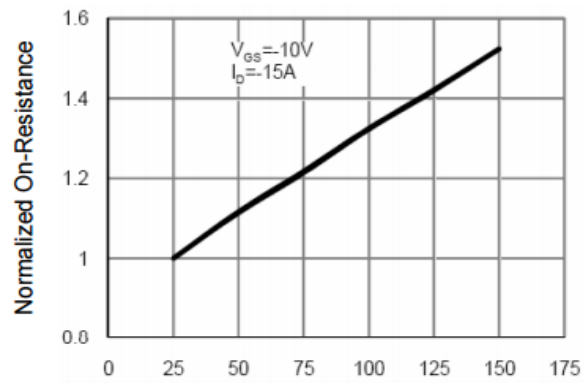
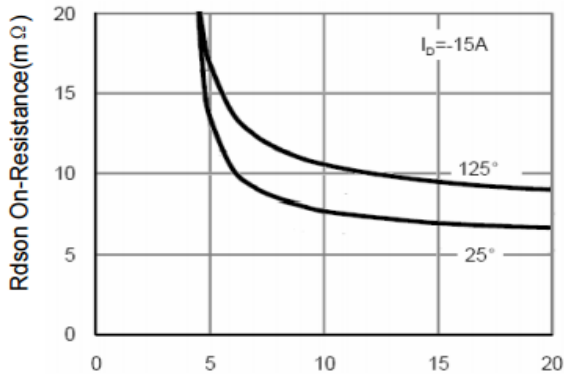
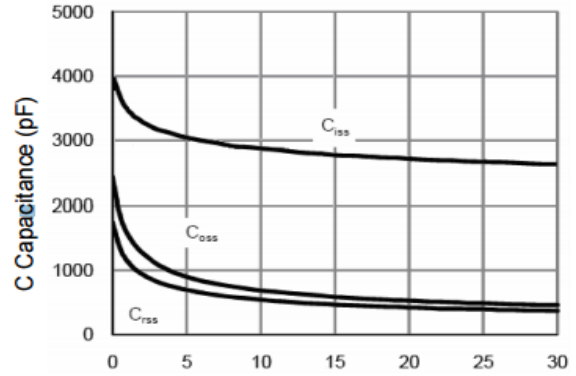


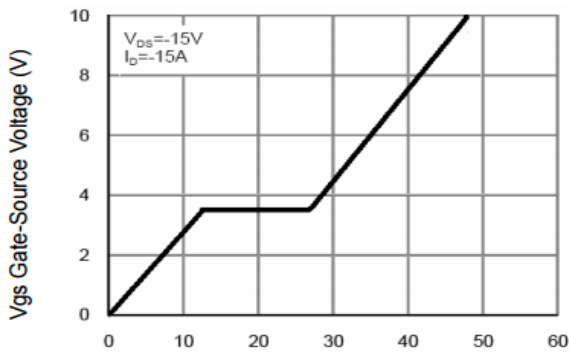
Figure 6 Drain-Source On-Resistance



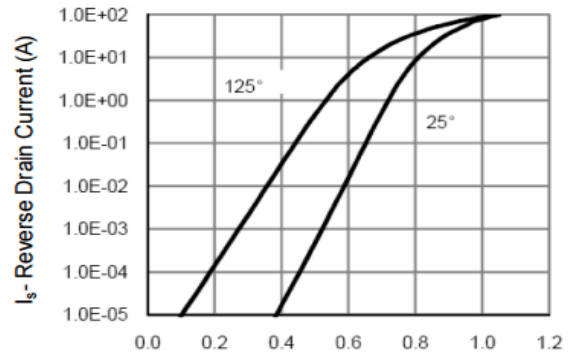
Vgs Gate-Source Voltage (V)
Figure 7 Rdson vs Vgs



Vds Drain-Source Voltage (V)
Figure 8 Capacitance vs Vds



Qg Gate Charge (nC)
Figure 9 Gate Charge



Vsd Source-Drain Voltage (V)
Figure 10 Source-Drain Diode Forward

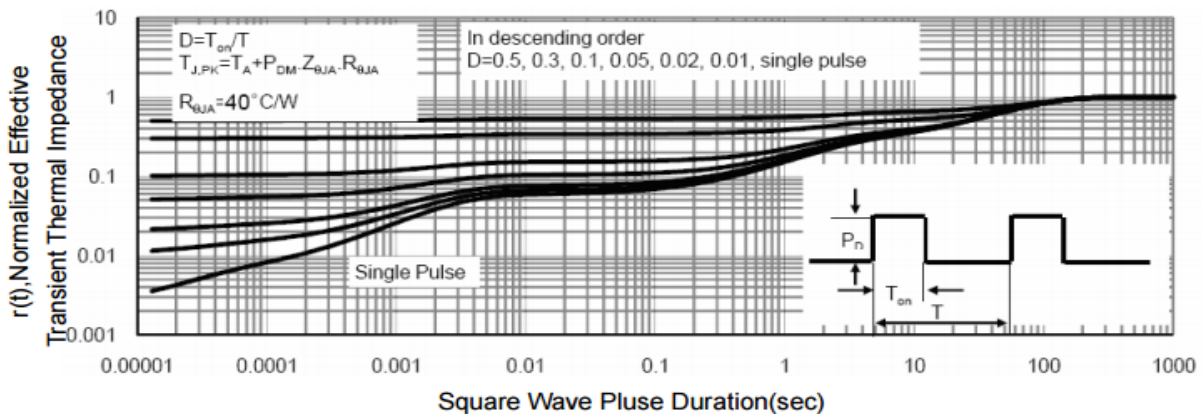
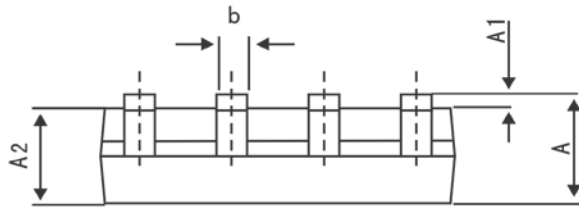
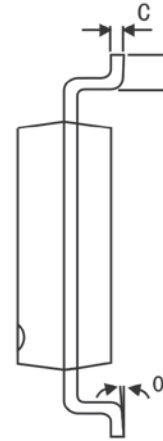
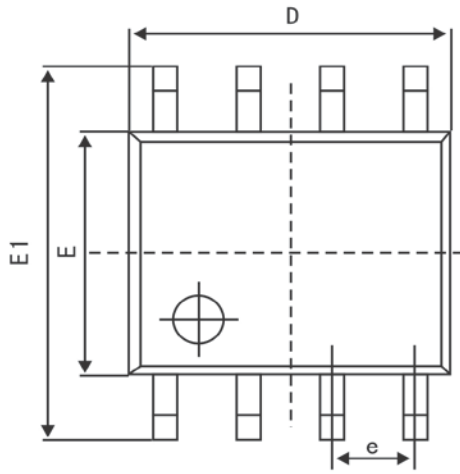


Figure 11 Normalized Maximum Transient Thermal Impedance

SOP-8 PACKAGE OUTLINE DIMENSIONS



Symbol	1.300	1.300	0.000	0.001
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°